## Remarks/Arguments:

Claims 1-18, 20 and 21 were pending in this patent application. Claims 20 and 21 are allowed. Claims 12, 14 and 17 are objected to. Claim 18 is cancelled without prejudice or disclaimer, thereby rendering moot the rejection under 35 USC 101.

A number of clarifying amendments have been made to the claims. In addition, some similar merely clarifying amendments have been made to allowed claim 20. No new matter has been added. Support for these amendments are found throughout the specification as filed, such as in paragraphs [0040] and [0042] of the corresponding published US application US2007/0280336 A1. For example, paragraph [0042] states in part:

> The second path 450 of the LMMSE-SIC receiver deviates from that of a conventional MIMO LMMSE receiver at least for the reason that the chip equalizer 455...does not attempt to directly generate the chip sequence from the second transmit antenna. Instead, it generates a weighted sum of the chip sequences...from both transmit antennas, while suppressing all the ICIs.

Filed herewith are a Supplemental Information Disclosure Statement and the required fee. The Supplemental Information Disclosure Statement makes of record a number of publications noted in the Background section and elsewhere in the US patent application.

Claims 1,2,4,7,9,13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Visotsky et al.. (US6175588) in view of Liang et al.. (US6314147). Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Visotsky et al. and Liang et al. in view of Diloisy (US7266355). Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Visotsky et al. and Liang et al. in view of Fukasawa et al. (US5533012). Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Visotsky et al. and Liang et al. in view of Wang et al. (US2020039391 ). Claims 10, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diloisy in view of Visotsky et al. and Liang et al. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Diloisy, Visotsky et al. and Liang et al. in view of Claussen et al.

These rejections are respectfully disagreed with and are traversed below.

In rejecting Claims 1,2,4,7,9,13, and 18 under 35 USC 103(a) the Examiner states that Visotsky et al. teach the claimed "second data path (the output of 218 to combiner 228 in fig. 2) for generating an estimated symbol sum $a_s(f)$ from said first and second inputs (fig. 2)."

The Examiner's interpretation of Visotsky et al. is respectfully disagreed with. What Visotsky et al. actually teach is the following (referring to col. 11, lines 11-61 and Figure 2):

> **Each of receiver circuit 201 and receiver circuit 203 operates similarly to receiver 100 in FIG. 1.** The sampler 202 converts the received spread spectrum signal to a discrete time signal at the sample rate, which is an integer multiple of the chip rate, such as one, two, four or eight times the chip rate. In the first receiver circuit 201, the adaptive equalizer 204 has an input 230 for receiving the spread spectrum signal and input 232 for receiving an error signal 234. The adaptive equalizer 204 suppresses interference on the spread spectrum signal to produce an equalized signal 236 at an output 238. The despreader 206 despreads the equalized signal 236 in response to a predetermined spreading sequence. **The traffic channel demodulator 208 demodulates the equalized, despread signal to produce an estimate of the data sequence transmitted on the traffic channel.** The traffic channel demodulator includes a despreader 240 and a summer 242. The despreader 240 despreads the equalized signal by applying the appropriate Walsh code for the traffic channel of interest. **The summer 242 sums chips over an interval, such as 64 chips, to produce a demodulated traffic channel.** The demodulated data is delayed by a predetermined time in the first delay element 212, multiplied by an appropriate gain in gain element 213, then passed to the combiner 228.
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> In the second receiver circuit 203, the adaptive equalizer 214 has an input 250 for receiving the sampled spread spectrum signal and input 252 for receiving the error signal 234. The adaptive equalizer 214 suppresses interference on the spread spectrum signal to produce an equalized signal 256 at an output 258. The despreader 216 despreads the equalized signal 256 in response to a predetermined spreading sequence. **The spreading sequences used by the first receiver circuit 201 and the second receiver circuit 203 correspond to particular base stations. In soft handoff, the each receiver circuit will be receiving signals from a different base station, so the spreading sequences will be different.** For example, in IS-95, the spreading sequences are different phases of a common sequence.
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> **The traffic channel demodulator 218 demodulates the equalized, despread signal to produce an estimate of the data sequence transmitted on the traffic channel. The traffic channel demodulator includes a despreader 260 and a summer 262.** The despreader 260 despreads the equalized signal by applying the appropriate Walsh code for the traffic channel of interest. **The summer 262 sums chips over an interval, such as 64 chips, to produce demodulated data.** The demodulated data is delayed by a predetermined time in the second delay element 222, multiplied by an appropriate gain in gain

> element 223, then passed to the combiner 228 for combination with the demodulated data from the first receiver circuit 201.

Clearly, in these passages from Visotsky et al. there is no disclosure of "a first input for coupling to a first receive antenna and a second input for coupling to a second receive antenna for receiving spread spectrum symbols from a transmitter having at least a first transmit antenna and a second transmit antenna". Only a single receive antenna is shown (Figure 4) and, in fact, the word "antenna" does not appear in Visotsky et al. In addition, there is no disclosure of receiving spread spectrum signals from a transmitter having at least a first transmit antenna and a second transmit antenna. Instead, signals are received from two separate transmitters (base stations), each apparently having a single transmit antenna (see, again, Figure 4).

As such, there is also clearly no disclosure of, or suggestion of:

> a second data path coupled to said first and second inputs and configured to generate an estimated symbol sum $\hat{a}_s(f)$ received from both the first transmit antenna and the second transmit antenna.

As was quoted above, instead Visotsky et al. disclose that in soft handoff "each receiver circuit will be receiving signals from a different base station". In Visotsky et al. there is clearly no estimated symbol sum that is generated from signals received from a first transmit antenna and a second transmit antenna of a transmitter.

This being the case, and even if Visotsky et al. were to be combined with Liang et al., which is not admitted is suggested or technically feasible, the resulting combination would clearly not disclose or suggest:

> an interference cancellation module having inputs coupled to the first and second data paths, said interference cancellation module **configured to cancel co-channel interference (CCI) between the estimated symbol sum and the first estimated symbol to generate a second estimated symbol.**

The linear space-time MMSE filter 140 of the CCI canceller 120 appears to operate on received signal samples from the receive antennas 80, and does not input an estimated symbol sum that is generated from signals received from a first transmit antenna and a second transmit antenna of a transmitter.

In that claim 1 is clearly patentable over the proposed combination of references, then for at least this one reason all claims that depend from claim 1 are also patentable whether considered only in view of Visotsky et al. in view of Liang et al., or also in view of the other cited references.

The arguments made above are applicable as well to method claim 13, which is also deemed to be allowable over the proposed combination of references, as are all claims dependent from claim 13.

The foregoing arguments are applicable as well to independent claims 10 and 15, which were rejected under 35 U.S.C. 103(a) as being unpatentable over Diloisy in view of Visotsky et al. and Liang et al. Note that claim 10 recites in part:

> a second chip equalizer having a first input coupled to said first receiver input and to second receiver input and a second input coupled to said second output of said channel estimator for **generating an estimated chip sequence sum for the signal received from the first transmit antenna and for a signal received from the second transmit antenna and a residual CCI**, said second chip equalizer having a first output coupled to a second processing module configured to descramble and despread the output of said second chip equalizer and to **generate an estimated symbol sum $\hat{a}_s(f)$**.

As was argued above, Visotsky et al. are not seen to expressly disclose or suggest this subject matter.

Claim 15 recites in part that an apparatus includes:

> means for **generating an estimated symbol sum $\hat{a}_s(f)$ for the signal received from the first transmit antenna and for a signal received from a second transmit antenna**;
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> means for **utilizing said first estimated symbol $\hat{a}_1(f)$ and said estimated symbol sum $\hat{a}_s(f)$ as a plurality of inputs to an interference cancellation module**, for canceling CCI and generating at least one estimated output symbol.

These claims, and all claims dependent thereon, should also be found to be in condition for allowance.

The Examiner is respectfully requested to reconsider and remove the expressed rejections, and to allow all of the pending claims as now presented for examination.

Respectfully submitted:

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